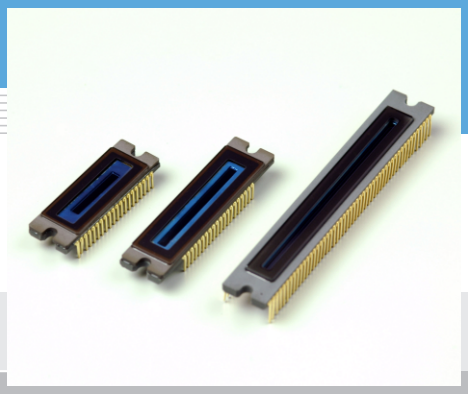


Back-thinned TDI-CCD

S10200-02, S10201-04, S10202-08, S10202-16



Operating the back-thinned CCD in TDI mode delivers high sensitivity.

TDI-CCD captures clear and bright images even under low-light-level conditions. During TDI mode, the CCD captures an image of a moving object while transferring integrated signal charges synchronously with the object movement. This operation mode dramatically boosts sensitivity to high levels even when capturing fast moving objects. Our new TDI-CCD uses the back-thinned structure to achieve even higher quantum efficiency over a wide spectral range from UV to near IR region (200 to 1100 nm).

Features

- TDI mode gives high sensitivity
- High-speed, continuous image acquisition
- Back-thinned structure ensures high sensitivity from UV to near IR
- Multiple ports for high-speed line rate

Applications

- Sequential imaging of high-speed moving samples
- Inspection tasks on electronic parts production line
- Semiconductor inspection
- Flow cytometry

TDI (Time Delay Integration) mode

In FFT-CCD, signal charges in each line are vertically transferred during charge readout. TDI mode synchronizes this vertical transfer timing with the movement of the object, so that signal charges are integrated a number of times equal to the number of vertical stages of the CCD pixels.

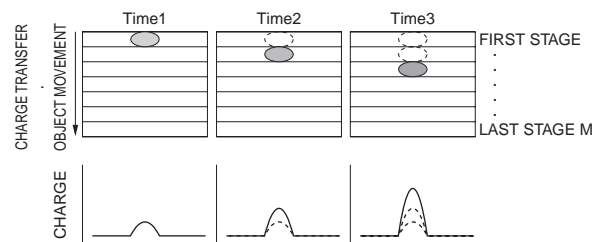
In the TDI mode, the signal charges must be transferred in the same direction at the same speed as those of the object to be imaged. These speeds are expressed by the following equation:

$$v = f \times d$$

v: Object moving speed, Charge transfer speed, f: Vertical transfer frequency, d: Pixel size

In the right figure, when the first stage charges are transferred to the second stage, an additional charges are produced in the second stage by photoelectric conversion and accumulated. When this operation is continuously repeated until reaching the last stage M (the number of vertical stages), signal charges which are M times greater than the initial charges are accumulated. Since the signal charges on each line are output from the CCD horizontal shift register, a two-dimensional image can be continuously acquired. In this way the TDI mode achieves sensitivity which is M times higher than linear image sensors (S/N is improved \sqrt{M} times). The TDI mode also improves sensitivity variations compared to frame mode operation.

- Schematic diagram showing integrated exposure by TDI mode



KMPDC0139EA

Selection guide

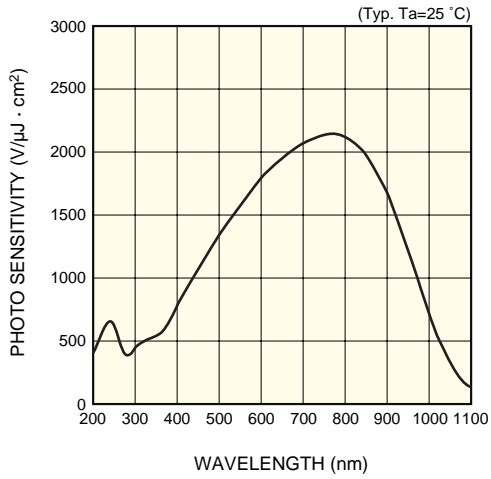
Type No.	Pixel size (μm)	Number of total pixels (H) × (V)	Number of active pixels (H) × (V)	Number of ports	Pixel rate (MHz/port)	Line rate (kHz)	Vertical transfer
S10200-02	12 × 12	1040 × 128	1024 × 128	2	30	50	Bidirectional
S10201-04		2080 × 128	2048 × 128	4			
S10202-08		4160 × 128	4096 × 128	8			
S10202-16		4224 × 128	4096 × 128	16		100	

Specifications

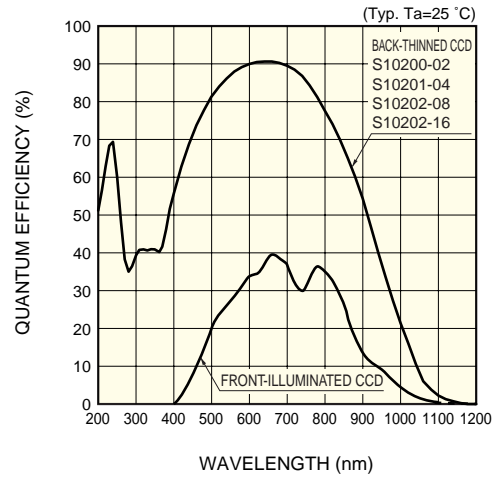
Parameter	Specification
TDI stage	128
Anti-blooming	FW × 100 (Min.)
Vertical clock	3 phases
Horizontal clock	2 phases
Output circuit	Two-stage MOSFET source follower
Package	Ceramic DIP
Window	Quartz glass



■ Spectral response (without window)



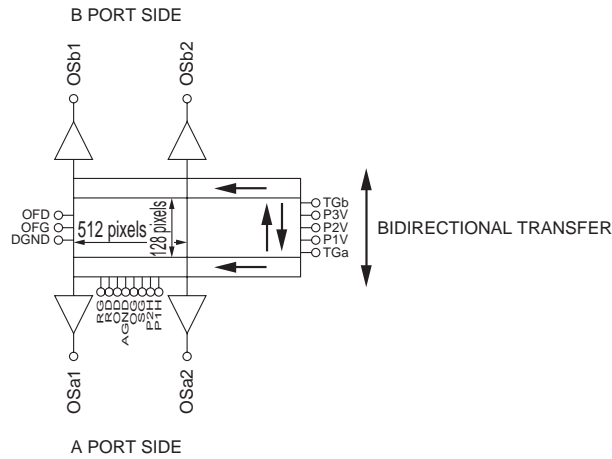
KMPDB0268EA



KMPDB0269EA

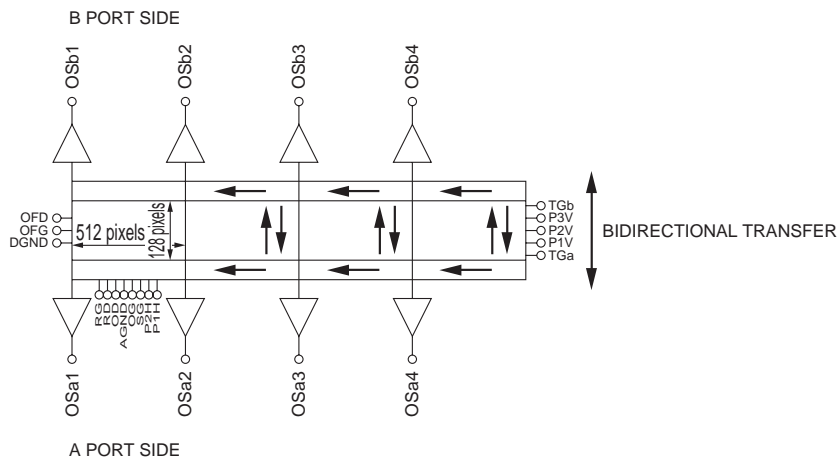
■ Sensor structure

S10200-02



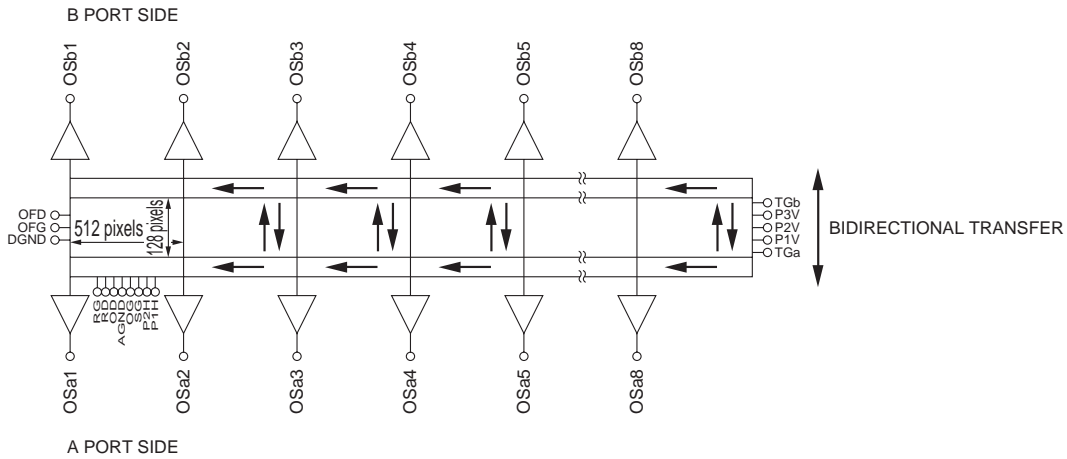
KMPDC0251EA

S10201-04

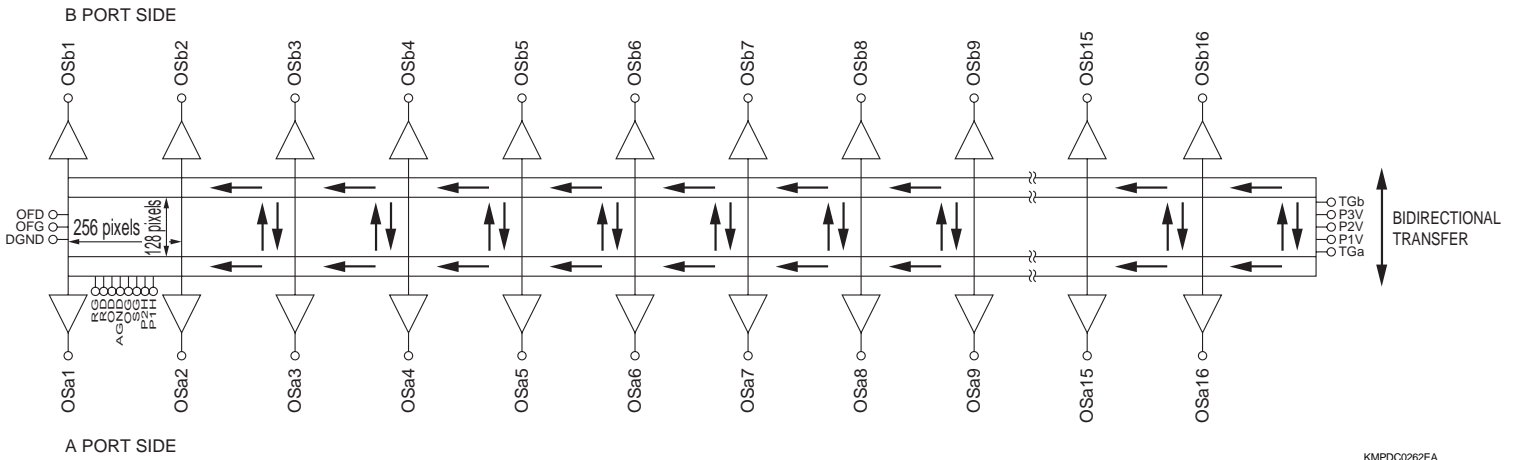


KMPDC0260EA

S10202-08



S10202-16



■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	60	°C
Storage temperature	Tstg	-50	-	70	°C
Output transistor drain voltage	VOD	-0.5	-	25	V
Reset drain voltage	VRD	-0.5	-	18	V
Overflow drain voltage	VOFD	-0.5	-	18	V
Overflow gate voltage	VOFG	-10	-	15	V
Summing gate voltage	VSG	-10	-	15	V
Output gate voltage	VOG	-10	-	15	V
Reset gate voltage	VRG	-10	-	15	V
Transfer gate voltage	VTG	-10	-	15	V
Vertical clock voltage	VP1V, VP2V, VP3V	-10	-	15	V
Horizontal clock voltage	VP1H, VP2H	-10	-	15	V

■ Operating conditions (TDI mode, Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Output transistor drain voltage	V _{OD}	12	15	18	V	
Reset drain voltage	V _{RD}	11	12	13	V	
Output gate voltage	V _{OG}	3	5	7	V	
Substrate voltage	V _{DGND} , V _{AGND}	-	0	-	V	
Overflow drain voltage	V _{OFD}	4	6	9	V	
Overflow gate voltage	V _{OFG}	0	4	6	V	
Vertical shift register clock voltage	High	VP1VH, VP2VH, VP3VH	4	6	8	V
	Low	VP1VL, VP2VL, VP3VL	-6	-5	-4	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	4	6	8	V
	Low	VP1HL, VP2HL	-6	-5	-4	
Summing gate voltage	High	V _{SGH}	4	6	8	V
	Low	V _{SHL}	-6	-5	-4	
Reset gate voltage	High	V _{RGH}	7	8	9	V
	Low	V _{RGL}	-6	0	-	
Transfer gate voltage	High	V _{TGH}	4	6	8	V
	Low	V _{TGL}	-6	-5	-4	

■ Electrical and optical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage	V _{sat}	-	FW × Sv	-	V
Full well capacity *1	FW	80	100	120	ke ⁻
CCD node sensitivity	Sv	3	3.5	4	μV/e ⁻
Dark current *1, *2	DS	-	100	300	e ⁻ /pixel
Readout noise *3	Nr	-	100	200	e ⁻ rms
Dynamic range	DR	-	1000	-	-
Photo response non-uniformity *4	PRNU	-	±3	±10	%
Spectral response range	λ	-	200 to 1100	-	nm

*1: TDI mode

*2: Line rate 50 kHz, accumulated dark signal after 128-stage transfer

*3: Readout frequency 30 MHz

*4: Measured at one-half of the full well. In TDI mode.

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Signal output frequency	fc	-	30	35	MHz	
Reset clock frequency	frg	-	30	35	MHz	
Vertical shift register capacitance	S10200-02	CP1V, CP2V, CP3V	-	250	-	pF
	S10201-04		-	400	-	
	S10202-08/-16		-	650	-	
Line rate	S10200-02	LR	-	50	-	kHz
	S10201-04		-	50	-	
	S10202-08		-	50	-	
	S10202-16		-	100	-	
Horizontal shift register capacitance	S10200-02	CP1H, CP2H	-	50	-	pF
	S10201-04		-	90	-	
	S10202-08/-16		-	90	-	
Transfer gate capacitance	S10200-02	CTG	-	40	-	pF
	S10201-04		-	60	-	
	S10202-08/-16		-	100	-	
Summing gate capacitance	S10200-02	CSG	-	20	-	pF
	S10201-04		-	40	-	
	S10202-08/-16		-	40	-	
Reset gate capacitance	S10200-02	CRG	-	20	-	pF
	S10201-04		-	40	-	
	S10202-08/-16		-	40	-	
Charge transfer efficiency *5	CTE	0.99995	0.99999	-	-	
Output level *6	V _{out}	-	6.5	-	V	
Output impedance *7	Z _o	-	300	-	Ω	
Output MOSFET supply current/node	I _{do}	-	5	10	mA	
Power consumption *6, *7	P	-	75	-	mW	

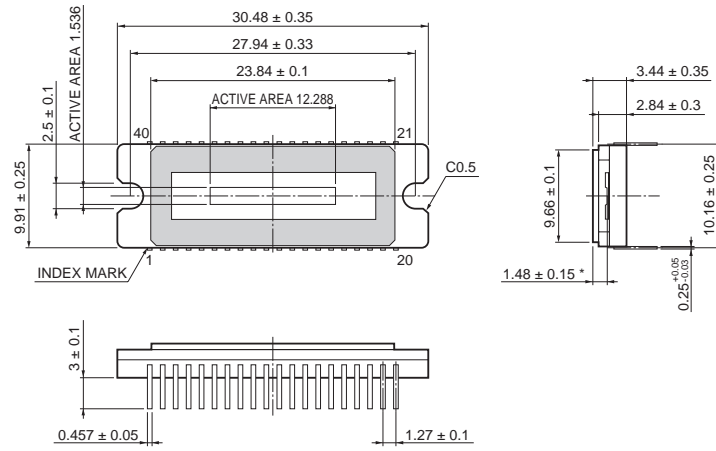
*5: Charge transfer efficiency per pixel, measured at half of the full well capacity.

*6: V_{OD}=15 V, Load resistance=2.2 kΩ

*7: Power consumption of the on-chip amplifier plus load resistance.

Dimensional outlines (unit: mm)

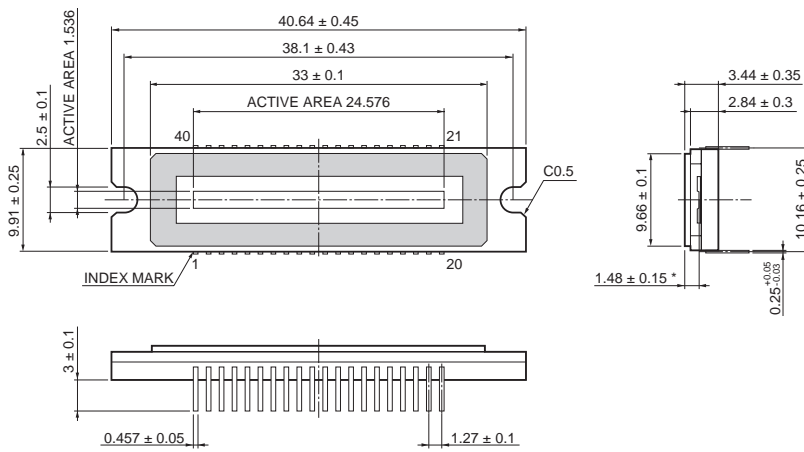
S10200-02



* Distance between window surface and photosensitive surface

KMPDA0218EB

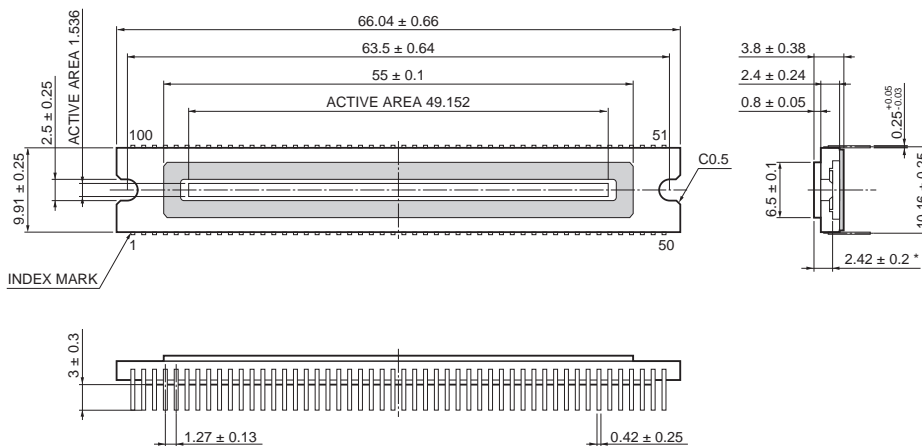
S10201-04



* Distance between window surface and photosensitive surface

KMPDA0219EB

S10202-08/-16



* Distance between window surface and photosensitive surface

KMPDA0220EB

■ Pin connections

S10200-02			S10201-04		
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	P2V	CCD vertical register clock-2	1	P2V	CCD vertical register clock-2
2	P3V	CCD vertical register clock-3	2	P3V	CCD vertical register clock-3
3	P1V	CCD vertical register clock-1	3	P1V	CCD vertical register clock-1
4	TGa	Transfer gate-a	4	TGa	Transfer gate-a
5	SSD	Digital GND	5	SSD	Digital GND
6	NC	No connection	6	OSa1	Output transistor source-a1
7	SSA	Analog GND	7	SSA	Analog GND
8	OSa1	Output transistor source-a 1	8	OSa2	Output transistor source-a2
9	OD1	Output drain-1	9	OD1	Output drain-1
10	OSa2	Output transistor source-a 2	10	OSa3	Output transistor source-a3
11	NC	No connection	11	OD3	Output drain-3
12	NC	No connection	12	OSa4	Output transistor source-a4
13	OG	Output gate	13	OG	Output gate
14	RD	Reset drain	14	RD	Reset drain
15	OFD	Overflow drain	15	OFD	Overflow drain
16	SSD	Digital GND	16	SSD	Digital GND
17	RGa	Reset gate-a	17	RGa	Reset gate-a
18	SGa	Summing gate-a	18	SGa	Summing gate-a
19	P1Ha	CCD horizontal register-a clock-1	19	P1Ha	CCD horizontal register-a clock-1
20	P2Ha	CCD horizontal register-a clock-2	20	P2Ha	CCD horizontal register-a clock-2
21	P2Hb	CCD horizontal register-b clock-2	21	P2Hb	CCD horizontal register-b clock-2
22	P1Hb	CCD horizontal register-b clock-1	22	P1Hb	CCD horizontal register-b clock-1
23	SGb	Summing gate-b	23	SGb	Summing gate-b
24	RGB	Reset gate-b	24	RGB	Reset gate-b
25	SSD	Digital GND	25	SSD	Digital GND
26	OFG	Overflow gate	26	OFG	Overflow gate
27	RD	Reset drain	27	RD	Reset drain
28	OG	Output gate	28	OG	Output gate
29	NC	No connection	29	Osb4	Output transistor source-b4
30	NC	No connection	30	OD4	Output drain-4
31	OSb2	Output transistor source-b2	31	Osb3	Output transistor source-b3
32	OD2	Output drain-2	32	OD2	Output drain-2
33	OSb1	Output transistor source-b1	33	OSb2	Output transistor source-b2
34	SSA	Analog GND	34	SSA	Analog GND
35	NC	No connection	35	OSb1	Output transistor source-b1
36	SSD	Digital GND	36	SSD	Digital GND
37	TGb	Transfer gate-b	37	TGb	Transfer gate-b
38	P1V	CCD vertical register clock-1	38	P1V	CCD vertical register clock-1
39	P3V	CCD vertical register clock-3	39	P3V	CCD vertical register clock-3
40	P2V	CCD vertical register clock-2	40	P2V	CCD vertical register clock-2

S10202-08					
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	P1Ha1	CCD horizontal register-a1 clock-1	51	P1Hb2	CCD horizontal register-b2 clock-1
2	P2Ha1	CCD horizontal register-a1 clock-2	52	P2Hb2	CCD horizontal register-b2 clock-2
3	SGa1	Summing gate-a1	53	SGb2	Summing gate-b2
4	RGa1	Reset gate-a1	54	RGB2	Reset gate-b2
5	SSD	Digital GND	55	SSD	Digital GND
6	SSA	Analog GND	56	SSA	Analog GND
7	OFG	Overflow gate	57	OFG	Overflow gate
8	OSa1	Output transistor source-a1	58	NC	No connection
9	OFD	Overflow drain	59	OFD	Overflow drain
10	NC	No connection	60	OSb8	Output transistor source-b8
11	RD	Reset drain	61	RD	Reset drain
12	OSa2	Output transistor source-a2	62	NC	No connection
13	OG	Output gate	63	OG	Output gate
14	NC	No connection	64	OSb7	Output transistor source-b7
15	OD1	Output drain-1	65	NC	No connection
16	OSa3	Output transistor source-a3	66	NC	No connection
17	NC	No connection	67	OD8	Output drain 8
18	NC	No connection	68	OSb6	Output transistor source-b6
19	OD3	Output drain-3	69	NC	No connection
20	OSa4	Output transistor source-a4	70	NC	No connection
21	NC	No connection	71	OD6	Output drain 6
22	NC	No connection	72	OSb5	Output transistor source-b5
23	SSD	Digital GND	73	SSD	Digital GND
24	TGa	Transfer gate-a	74	P1V	CCD vertical register clock-1
25	P2V	CCD vertical register clock-2	75	P3V	CCD vertical register clock-3
26	P3V	CCD vertical register clock-3	76	P2V	CCD vertical register clock-2
27	P1V	CCD vertical register clock-1	77	TGb	Transfer gate-b
28	SSD	Digital GND	78	SSD	Digital GND
29	OSa5	Output transistor source-a5	79	NC	No connection
30	OD5	Output drain-5	80	NC	No connection
31	NC	No connection	81	OSb4	Output transistor source-b4
32	NC	No connection	82	OD4	Output drain 4
33	OSa6	Output transistor source-a6	83	NC	No connection
34	OD7	Output drain-7	84	NC	No connection
35	NC	No connection	85	OSb3	Output transistor source-b3
36	NC	No connection	86	OD2	Output drain 2
37	OSa7	Output transistor source-a7	87	NC	No connection
38	OG	Output gate	88	OG	Output gate
39	NC	No connection	89	OSb2	Output transistor source-b2
40	RD	Reset drain	90	RD	Reset drain
41	OSa8	Output transistor source-a8	91	NC	No connection
42	OFD	Overflow drain	92	OFD	Overflow drain
43	NC	No connection	93	OSb1	Output transistor source-b1
44	OFG	Overflow gate	94	OFG	Overflow gate
45	SSA	Analog GND	95	SSA	Analog GND
46	SSD	Digital GND	96	SSD	Digital GND
47	RGa2	Reset gate-a2	97	RGB1	Reset gate-b2
48	SGa2	Summing gate-a2	98	SGb1	Summing gate-b2
49	P2Ha2	CCD horizontal register-a2 clock-2	99	P2Hb1	CCD horizontal register-b1 clock-2
50	P1Ha2	CCD horizontal register-a2 clock-1	100	P1Hb1	CCD horizontal register-b1 clock-1

S10202-16					
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	P1Ha1	CCD horizontal register-a1 clock-1	51	P1Hb2	CCD horizontal register-b2 clock-1
2	P2Ha1	CCD horizontal register-a1 clock-2	52	P2Hb2	CCD horizontal register-b2 clock-2
3	SGa1	Summing gate-a1	53	SGb2	Summing gate-b2
4	RGa1	Reset gate-a1	54	RGB2	Reset gate-b2
5	SSD	Digital GND	55	SSD	Digital GND
6	SSA	Analog GND	56	SSA	Analog GND
7	OFG	Overflow gate	57	OFG	Overflow gate
8	OSa1	Output transistor source-a1	58	OSb16	Output transistor source-b16
9	OFD	Overflow drain	59	OFD	Overflow drain
10	OSa2	Output transistor source-a2	60	OSb15	Output transistor source-b15
11	RD	Reset drain	61	RD	Reset drain
12	OSa3	Output transistor source-a3	62	OSb14	Output transistor source-b14
13	OG	Output gate	63	OG	Output gate
14	OSa4	Output transistor source-a4	64	OSb13	Output transistor source-b13
15	OD1	Output drain-1	65	OD16	Output drain-16
16	OSa5	Output transistor source-a5	66	OSb12	Output transistor source-b12
17	OD2	Output drain-2	67	OD15	Output drain-15
18	OSa6	Output transistor source-a6	68	OSb11	Output transistor source-b11
19	OD5	Output drain-5	69	OD12	Output drain-12
20	OSa7	Output transistor source-a7	70	OSb10	Output transistor source-b10
21	OD6	Output drain-6	71	OD11	Output drain-11
22	OSa8	Output transistor source-a8	72	OSb9	Output transistor source-b9
23	SSD	Digital GND	73	SSD	Digital GND
24	TGa	Transfer gate-a	74	P1V	CCD vertical register clock-1
25	P2V	CCD vertical register clock-2	75	P3V	CCD vertical register clock-3
26	P3V	CCD vertical register clock-3	76	P2V	CCD vertical register clock-2
27	P1V	CCD vertical register clock-1	77	TGb	Transfer gate-b
28	SSD	Digital GND	78	SSD	Digital GND
29	OSa9	Output transistor source-a9	79	OSb8	Output transistor source-b8
30	OD9	Output drain-9	80	OD8	Output drain-8
31	OSa10	Output transistor source-a10	81	OSb7	Output transistor source-b7
32	OD10	Output drain-10	82	OD7	Output drain-7
33	OSa11	Output transistor source-a11	83	OSb6	Output transistor source-b6
34	OD13	Output drain-13	84	OD4	Output drain-4
35	OSa12	Output transistor source-a12	85	OSb5	Output transistor source-b5
36	OD14	Output drain-14	86	OD3	Output drain-3
37	OSa13	Output transistor source-a13	87	OSb4	Output transistor source-b4
38	OG	Output gate	88	OG	Output gate
39	OSa14	Output transistor source-a14	89	OSb3	Output transistor source-b3
40	RD	Reset drain	90	RD	Reset drain
41	OSa15	Output transistor source-a15	91	OSb2	Output transistor source-b2
42	OFD	Overflow drain	92	OFD	Overflow drain
43	OSa16	Output transistor source-a16	93	OSb1	Output transistor source-b1
44	OFG	Overflow gate	94	OFG	Overflow gate
45	SSA	Analog GND	95	SSA	Analog GND
46	SSD	Digital GND	96	SSD	Digital GND
47	RGa2	Reset gate-a2	97	RGB1	Reset gate-b1
48	SGa2	Summing gate-a2	98	SGb1	Summing gate-b1
49	P2Ha2	CCD horizontal register-a2 clock-2	99	P2Hb1	CCD horizontal register-b1 clock-2
50	P1Ha2	CCD horizontal register-a2 clock-1	100	P1Hb1	CCD horizontal register-b1 clock-1

■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk, etc. that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

TDI camera C10000 series

The TDI camera C10000 series is useful in a wide range of imaging applications that require both high speed and high sensitivity, including in-line monitoring and inspection.



■ Specifications

Parameter	C10000-301	C10000-401
Pixel number	1024 (H) × 128 (V)	2048 (H) × 128 (V)
Device structure	Back-thinned type	
Pixel size	12 μm (H) × 12 μm (V)	
Effective area	12.29 mm (H) × 1.536 mm (V)	24.58 mm (H) × 1.536 mm (V)
TDI transfer direction	Bi direction	
Readout mode	TDI readout mode or Frame readout mode *9	
TDI output channel	2 ports (512 × 2)	4 ports (512 × 4)
Anti-blooming	Lateral overflow drain (× 100)	
TDI pixel clock rate	30 MHz	
TDI line rate	0.45 kHz to 50 kHz	
Full-well capacity (Typ.)	100 000 electrons	
Readout noise (Typ.)	150 electrons rms	
Dynamic range (Typ.)	667 : 1	
A/D converter	12-bit	
Image processing	Real-time shading correction with internal DSP	
Lens mount	C-mount	F-mount
Interface	Base configuration	
Camera output clock	60 MHz	
Camera output channel	1 port (1024 × 1)	2 ports (1024 × 2)
TDI line rate control	Internal setting by serial command *10 External trigger	
Analog enhancement gain	1 time to 5 times (16 steps)	
Power / Power consumption	DC +12 V / 21 V · A	
Camera control	Serial control in Camera link	

*9: Frame readout mode is useful for easy focusing, but it is not suitable for measurement.

Please consult with our sales office for details.

*10: Internal TDI line rate can be set in 33 ns steps.

Note: Guaranteed linearity is up to 80000 electrons.

HAMAMATSU

Information furnished by HAMAMATSU is believed to be reliable. However, no responsibility is assumed for possible inaccuracies or omissions. Specifications are subject to change without notice. No patent rights are granted to any of the circuits described herein. ©2008 Hamamatsu Photonics K.K.

HAMAMATSU PHOTONICS K.K., Solid State Division

1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184, www.hamamatsu.com

U.S.A.: Hamamatsu Corporation: 360 Foothill Road, P.O.Box 6910, Bridgewater, N.J. 08807-0910, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218

Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 08152-3750, Fax: (49) 08152-2658

France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10

United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777

North Europe: Hamamatsu Photonics Norden AB: Smidesvägen 12, SE-171 41 Solna, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01

Italy: Hamamatsu Photonics Italia S.R.L.: Strada della Moia, 1/E, 20020 Arese, (Milano), Italy, Telephone: (39) 02-935-81-733, Fax: (39) 02-935-81-741